19-3982; Rev 0; 10/07

EVALUATION KIT AVAILABLE

Highly Integrated, 25A, Wide-Input, Internal MOSFET, Step-Down Regulator

General Description

The MAX8655 synchronous-PWM buck regulator operates from a 4.5V to 25V input and generates an output voltage adjustable from 0.7V to 5.5V at loads up to 25A. Integrated power MOSFETs provide a small footprint, ease of layout, and reduced EMI. Removing the board trace inductances ensures the highest efficiency at high frequency.

The MAX8655 uses peak current-mode control architecture with an adjustable (200kHz to 1MHz), constant-switching frequency, which is externally synchronizable. The MAX8655's adjustable current limit uses the inductor's DC resistance to improve efficiency or an external sense resistor for higher accuracy. Foldback type current limit is available to reduce the power dissipation under severe-overload or short-circuit conditions. A reference input is provided for use with a high-accuracy external reference or for DDR and tracking applications.

Monotonic startup provides safe starting into a prebiased output, where traditional step-down regulators discharge the output capacitor during soft-start, creating a negative voltage at the output and possibly damaging the load.

A 180° out-of-phase synchronization output is available for synchronizing with another MAX8655.

An enable input is provided for on/off control and to facilitate output sequencing. Output-voltage sensing for programmable overvoltage protection is provided and is independent of the feedback network to further enhance the output overvoltage protection.

Overall, the MAX8655 provides enough flexibility for the experienced user, as well as simplicity and ease of use for non-power-supply engineers.

Applications

Point-of-Load Power Supplies
Telecom Power
Networking
Nonisolated DC-DC Power Modules
Servers and Workstations
Notebook Computers
IBA Power Supplies

Ordering Information

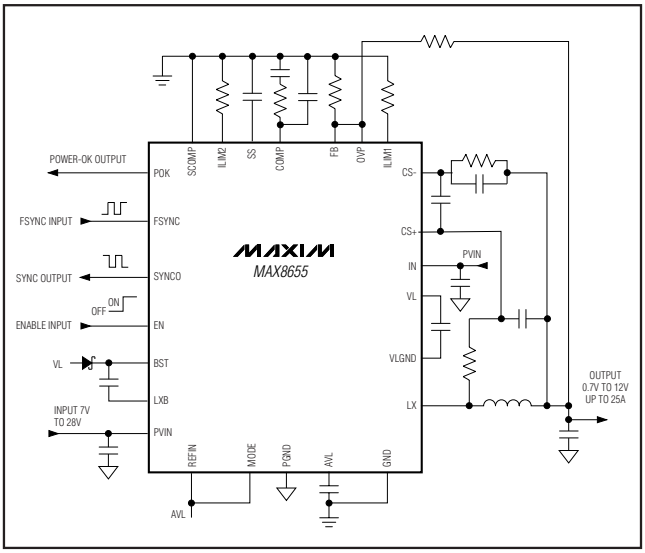
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8655ETN+	-40°C to +85°C	56 TQFN-EP* (8mm x 8mm)	T5688M-4

+Denotes a lead-free package.
**EP = Exposed pad.*

Features

- ♦ **25A Output Current**
- ♦ **Integrated Power MOSFETs**
- ♦ **Operates from 4.5V to 25V Supply**
- ♦ **1% FB Voltage Accuracy Over Temperature**
- ♦ **Adjustable Output Voltage Down to 0.7V**
- ♦ **Adjustable Switching Frequency and External Synchronization from 200kHz to 1MHz**
- ♦ **Multiphase Operation with Accurate Current Sharing**
- ♦ **180° Phase-Shifted Synchronization**
- ♦ **Adjustable Overcurrent Limit**
- ♦ **Adjustable Slope Compensation**
- ♦ **Selectable Current-Limit Mode: Latch-Off or Automatic Recovery**
- ♦ **Monotonic Output Voltage Rise at Startup into Prebias Output**
- ♦ **Output Sources and Sinks Current for DDR Applications**
- ♦ **Enable Input**
- ♦ **Power-OK (POK) Output**
- ♦ **Adjustable Soft-Start**
- ♦ **Independently Adjustable Overvoltage Protection**

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

PVIN, IN, EN to GND .....-0.3V to +30V
BST to LXB .....-0.3V to +7.5V
LX, LXB to GND..... (-2.5V for < 50ns transient) -1V to +30V
ILIM2, ILIM1, SYNCO, FSYNC, OVP, SCOMP to GND .....-0.3V to (V_{AVL} + 0.3V)
VL to PGND .....-0.3V to +7.5V
AVL, FB, POK, COMP, SS, MODE, REFIN to GND ..-0.3V to +6V
CS+, CS- to GND .....-0.3V to +6V
PGND to GND to VLGND .....-0.3V to +0.3V
Operating Junction Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
θ_{JC} (thermal resistance from junction to exposed pad) (Note 1) .....3.5°C/W
θ_{JT} (thermal resistance from junction to the top) .....3.9°C/W
$I_{LX\ (RMS)}$ 27A
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, see **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{BST} - V_{LX} = 6.5V, T_A = -40°C to +85°C, circuit of Figure 4, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PVIN Operating Voltage Range		3		25	V
IN Operating Voltage Range	VL = IN for V_{IN} < 7V	4.5		25.0	V
IN Quiescent Supply Current	V_{FB} = 0.75V, no switching		2	3	mA
Shutdown Supply Current	EN = GND, V_{IN} ≤ 28V			10	µA
	I_{IN} + I_{VL} + I_{AVL}, EN = GND, V_{AVL} = V_{VL} = V_{IN} = 5V			32	
PVIN Shutdown Supply Current	V_{PVIN} = V_{LX} = V_{BST}		1		µA
AVL Undervoltage-Lockout Threshold	V_{AVL} rising, 3% typical hysteresis	3.90	4.15	4.40	V
Output-Voltage Adjust Range	Minimum output voltage is limited by minimum duty cycle and external components	0.7		5.5	V
VL Regulation Voltage	7V < V_{IN} < 28V	6.0	6.5	7.0	V
AVL Regulation Voltage	5.5V < V_{VL} < 7V, 1mA < I_{LOAD} < 10mA	4.900	4.975	5.050	V
AVL Output Current		10			mA
SOFT-START					
SS Shutdown Resistance	From SS to GND, V_{EN} = 0V		20	100	Ω
SS Soft-Start Current	V_{REF} = 0.625V	18	23	28	µA
REFIN INPUT					
REFIN Dual Mode™ Threshold		V_{AVL} - 1.0V		V_{AVL}	V
REFIN Input Bias Current	V_{REFIN} = 0.7V to 1.5V	-250		+250	nA
REFIN Input Voltage Range		0		1.5	V

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{BST} - V_{LX} = 6.5V, T_A = -40°C to +85°C, circuit of Figure 4, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ERROR AMPLIFIER						
FB Regulation Voltage	REFIN = AVL		0.693	0.7	0.707	V
	V_{REFIN} = 0.7V to 1.5V		V_{REFIN} - 0.00375	V_{REFIN}	V_{REFIN} + 0.00375	
Transconductance			70	110	160	µS
COMP Shutdown Resistance	From COMP to GND, V_{EN} = 0V			20	100	Ω
FB Input Leakage Current	V_{FB} = 0.7V			5	50	nA
FB Input Common-Mode Range			-0.1		+1.5	V
CURRENT-SENSE AMPLIFIER						
Voltage Gain	V_{CS+} - V_{CS-} = 30mV	V_{OUT} = 0 to 5.5V		12		V/V
		Part to part variation at T_A = +85°C	-4		+4	%
CURRENT LIMIT						
Peak Current-Limit Threshold (V_{CS+} - V_{CS-})	R_{ILIM1} = 24kΩ		27.2	32	36.8	mV
	ILIM1 = AVL		60	80	92	
Negative Current Limit	% of valley current limit		-90	-120	-150	%
CS+, CS- Input Bias Current	V_{CS+} = V_{CS-} = 0 or 5.5V		-25		+25	µA
CS+, CS- Input Common-Mode Range			0		5.5	V
SLOPE COMPENSATION						
Slope Compensation at Maximum Duty Cycle	V_{SCOMP} = 2.5V		231.25	250.00	268.75	mV
	V_{SCOMP} = 1.25V		113.77	123.00	132.23	
	SCOMP = AVL		231.25	250.00	268.75	
	SCOMP = GND	T_A = 0°C to +85°C	113.77	123.00	132.23	
		T_A = -40°C to +85°C	110.70	123.00	132.23	
SCOMP High Threshold					V_{AVL} - 0.5	V
SCOMP Low Threshold			0.5			V
SCOMP Adjustment Range			1.25		2.50	V
SCOMP Input Leakage Current	V_{SCOMP} = 1.25V to 2.5V			5	200	nA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{BST} - V_{LX} = 6.5V, T_A = -40°C to +85°C, circuit of Figure 4, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

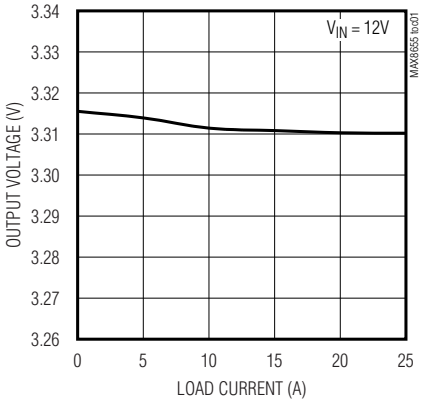
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Switching Frequency	R_{FSYNC} = 21.0kΩ	800	1000	1200	kHz
	R_{FSYNC} = 143kΩ	160	200	240	
Minimum Off-Time	Measured at LX		235		ns
Minimum On-Time	Measured at LX		75	100	ns
FSYNC Synchronization Range		160		1200	kHz
FSYNC Input High Pulse Width		100			ns
FSYNC Input Low Pulse Width		100			ns
FSYNC Rise/Fall Time				100	ns
SYNCO Phase Shift			180		Degrees
SYNCO Output Low Level	I_{SYNCO} = 5mA			0.4	V
SYNCO Output High Level	I_{SYNCO} = -5mA	V_{AVL} - 1V			V
FSYNC Input Low				0.4	V
FSYNC Input High		2.5			V
THERMAL PROTECTION					
Thermal Shutdown	Rising temperature		+160		°C
Thermal-Shutdown Hysteresis			15		°C
POK					
POK Threshold	REFIN = AVL, V_{FB} rising, typical hysteresis is 3%	629	650	671	mV
	V_{REFIN} = 0.75V to 1.5V, V_{FB} rising, typical hysteresis is 3%	88.7	91.7	94.7	%
POK Output Voltage, Low	V_{FB} = 0.6V, I_{POK} = 2mA		25	200	mV
POK Leakage Current, High	V_{POK} = 5.5V			1	µA
OVP					
OVP Threshold Voltage	REFIN = AVL	770	800	840	mV
	V_{REFIN} = 0.7V to 1.5V	110	115	120	%
OVP, Leakage Current, High	V_{OVP} = 0.8V			500	nA
MODE CONTROL					
MODE Logic-Level Low	4.5V ≤ V_{AVL} ≤ 5.5V			0.4	V
MODE Logic-Level High	4.5V ≤ V_{AVL} ≤ 5.5V	1.8			V
MODE Input Current	V_{MODE} = 0 to V_{AVL}	-1		+1	µA
SHUTDOWN CONTROL					
EN Logic-Level Low	4.5V ≤ V_{AVL} ≤ 5.5V			0.45	V
EN Logic-Level High	4.5V ≤ V_{AVL} ≤ 5.5V	2			V
EN Input Current	V_{EN} = 0V	-1		+1	µA
	V_{EN} = 28V		1.5	6.0	

Note 2: Specifications are 100% production tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design.

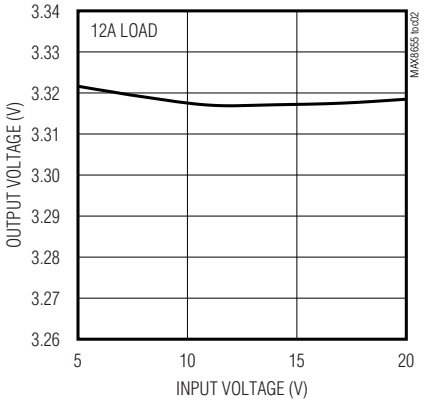
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

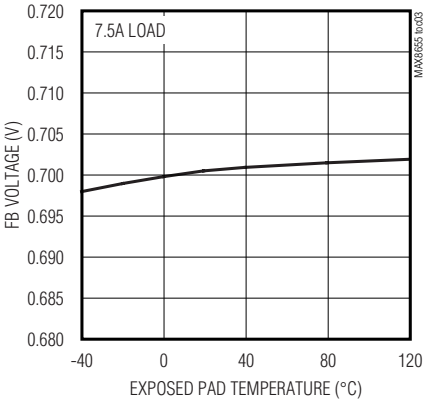
LOAD REGULATION (CIRCUIT OF FIGURE 4)



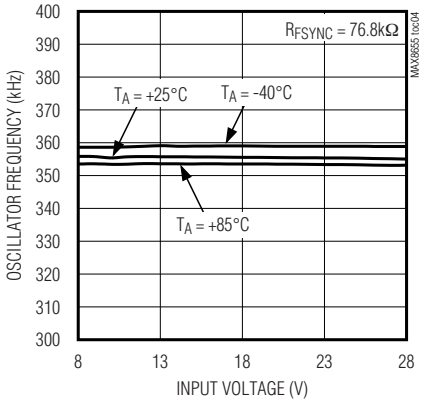
LINE REGULATION (CIRCUIT OF FIGURE 4)



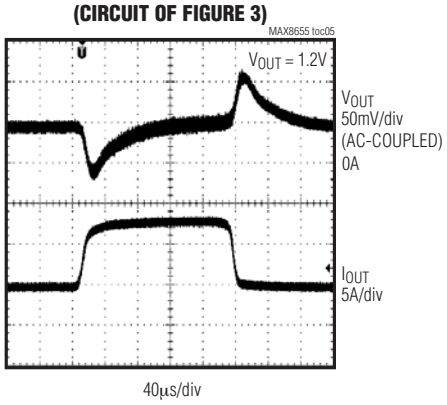
FB VOLTAGE vs. EXPOSED PAD TEMPERATURE (CIRCUIT OF FIGURE 4)



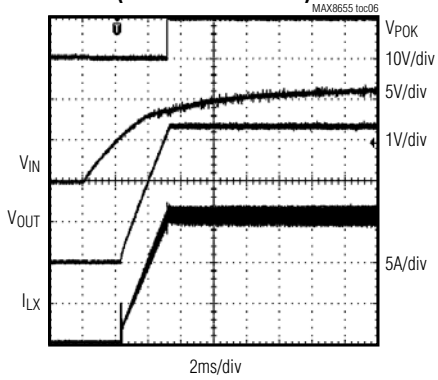
OSCILLATOR FREQUENCY vs. INPUT VOLTAGE (CIRCUIT OF FIGURE 4)



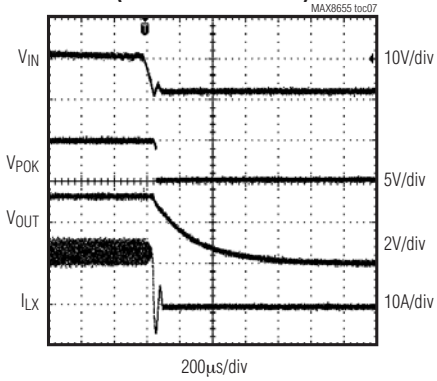
STEP-LOAD RESPONSE (CIRCUIT OF FIGURE 3)



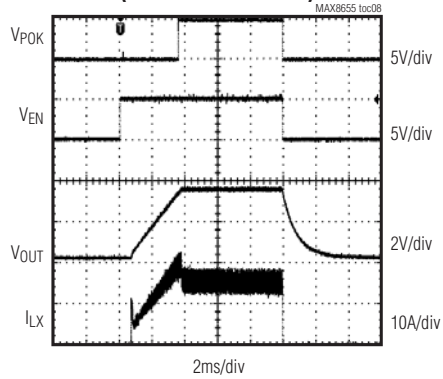
POWER-UP WAVEFORMS (CIRCUIT OF FIGURE 4)



POWER-DOWN WAVEFORMS (CIRCUIT OF FIGURE 4)



ENABLE WAVEFORMS (CIRCUIT OF FIGURE 4)

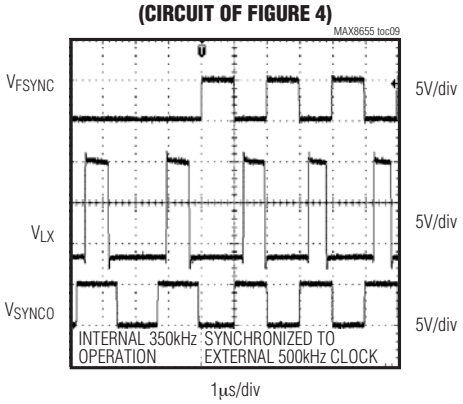


Highly Integrated, 25A, Wide-Input, Internal MOSFET, Step-Down Regulator

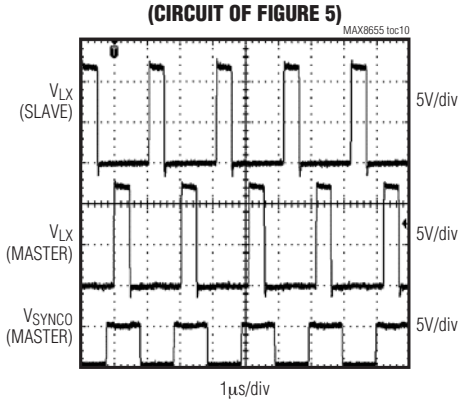
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

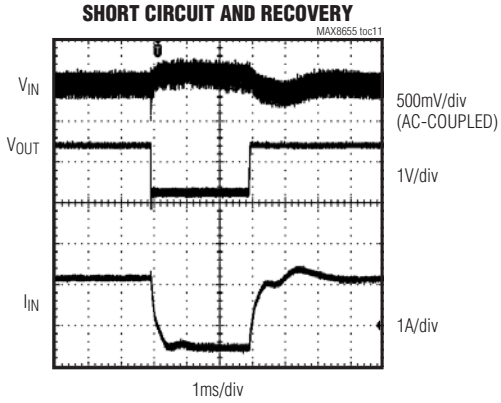
FSYNC AND SYNCO (CIRCUIT OF FIGURE 4)



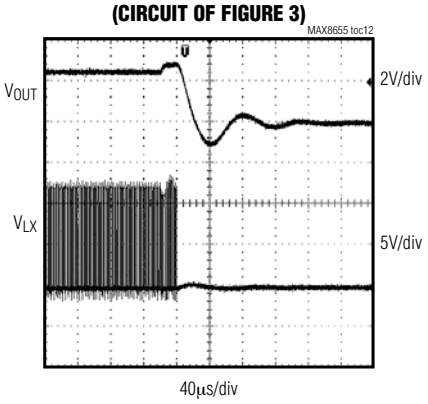
DUAL-PHASE SWITCHING (CIRCUIT OF FIGURE 5)



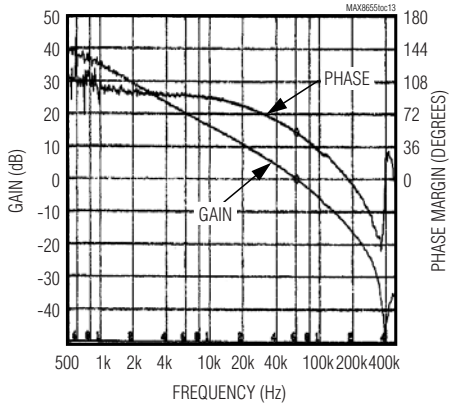
SHORT CIRCUIT AND RECOVERY



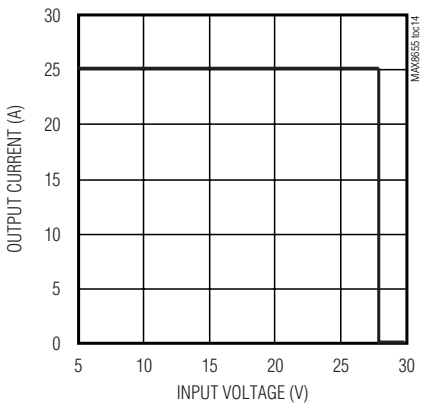
OVERVOLTAGE PROTECTION (CIRCUIT OF FIGURE 3)



CLOSED-LOOP BODE PLOT (CIRCUIT OF FIGURE 3)



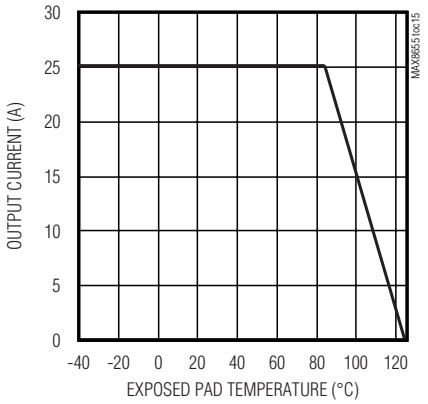
SAFE OPERATING AREA



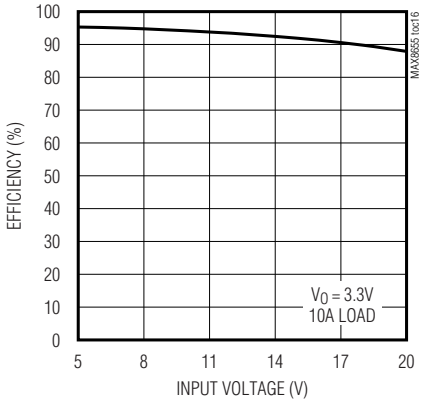
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

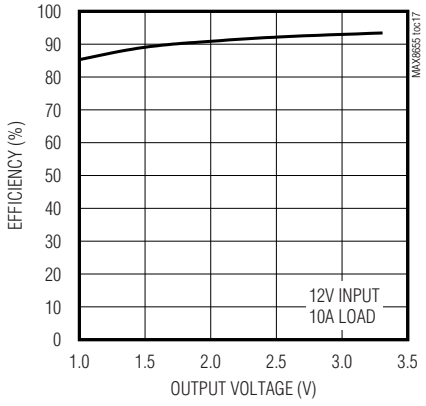
MAXIMUM OUTPUT CURRENT vs. EXPOSED PAD TEMPERATURE (CIRCUIT OF FIGURE 4)



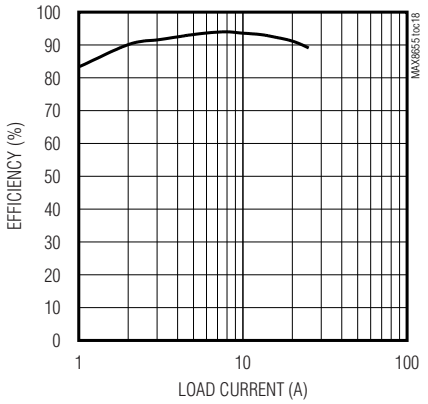
EFFICIENCY vs. INPUT VOLTAGE (CIRCUIT OF FIGURE 4)



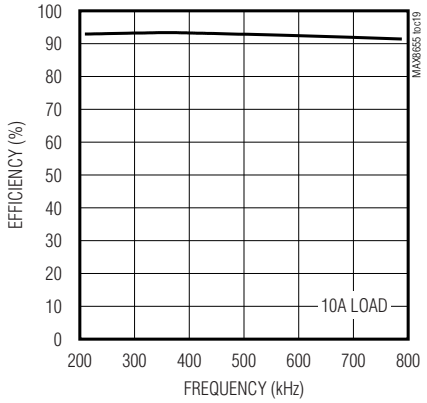
EFFICIENCY vs. OUTPUT VOLTAGE (CIRCUIT OF FIGURE 4)



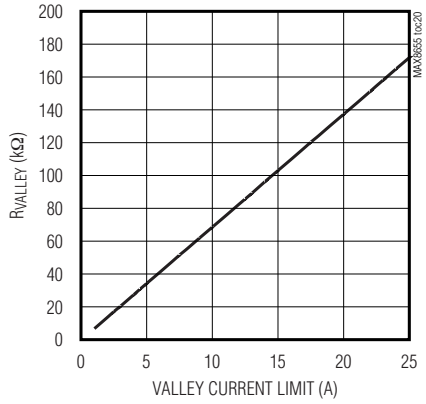
EFFICIENCY vs. LOAD CURRENT 12V INPUT, 3.3V OUTPUT (CIRCUIT OF FIGURE 4)



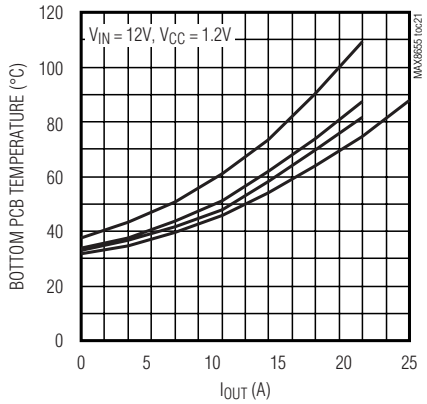
EFFICIENCY vs. FREQUENCY 12.0V INPUT 3.3V OUTPUT (CIRCUIT OF FIGURE 4)



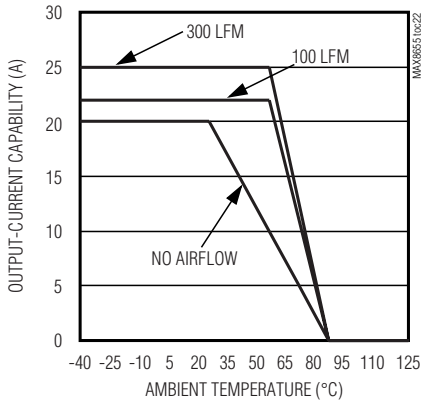
R_{VALLEY} vs. VALLEY CURRENT LIMIT



BOTTOM LAYER PCB TEMPERATURE vs. OUTPUT CURRENT



OUTPUT-CURRENT CAPABILITY vs. AMBIENT TEMPERATURE



Highly Integrated, 25A, Wide-Input, Internal MOSFET, Step-Down Regulator

Pin Description

PIN	NAME	FUNCTION
1–5, 51–56	PVIN	Power-Input Supply. PVIN connects to the drain of the internal high-side MOSFET. Connect input-decoupling capacitors as close as possible between PVIN and PGND.
6, 16–21	LX	External Inductor Connection. Connect to the external power inductor. Leave pin 6 unconnected for best routing.
7–15	PGND	Power Ground Connection from Source of Internal Low-Side MOSFET. Connect input-decoupling capacitors as close as possible between PVIN and PGND.
22	VLGND	Return for Low-Side MOSFET Gate-Driver Current
23, 28, 39, 48	GND	Analog Ground. Connect all pins to the analog ground plane, and connect the analog and power ground planes together at the negative terminal of the output capacitor. Low-current signals return to GND. Pin 28 must be connected externally to GND-EP, the analog ground plane.
24	VL	Internal 6.5V Linear-Regulator Output. Connect a 2.2µF to 10µF ceramic capacitor from VL to VLGND. For V_{IN} < 7V, connect VL directly to IN. VL supplies power for the internal gate drivers. VL is the input to the AVL internal linear regulator.
25	IN	Input Supply Voltage. IN is the input to the VL linear regulator. Connect VL to IN for V_{IN} < 7V. Decouple to PGND with a 0.22µF ceramic capacitor.
26	EN	Enable. Apply logic-high to EN to enable the output, or logic-low to place the regulator in low-power shutdown mode. Connect EN to IN for always-on operation.
27	AVL	Internal 5V Linear-Regulator Output. AVL powers the MAX8655's internal circuits. Connect a 1µF ceramic capacitor from AVL to GND.
29, 30, 42, 49	N.C.	No Connection. Not internally connected.
31	CS+	Positive Differential Current-Sense Input
32	CS-	Negative Differential Current-Sense Input
33	ILIM1	Analog Programmable Current-Limit Input for Inductor Current. Connect a resistor from ILIM1 to GND to set the overcurrent threshold. ILIM1 sources 10µA through the resistor, and the voltage at ILIM1 is attenuated 7.5:1 to set the final current limit. For example, a 60kΩ resistor results in 600mV at ILIM1. This results in a current-limit threshold (V_{CS+} - V_{CS-}) of 80mV. The ILIM1 resistor range is 24kΩ to 60kΩ. Connect ILIM1 to AVL to set the default threshold of 80mV.
34	OVP	Output-Voltage Sensing for Overvoltage Protection. Connect OVP to the center of a resistor-divider connected between the output of the regulator and GND to set the FB independent output overvoltage trip point. Connect OVP to FB if this independence is not desired. The OVP threshold is 1.15 times the nominal feedback regulation voltage.
35	FB	Feedback Input. Connect FB to the center of a resistor voltage-divider connected between the output and GND to set the output voltage. FB regulates to 0.7V or V_{REFIN}.
36	COMP	Loop Compensation. Connect COMP to an external RC network to compensate the loop. COMP is internally pulled to GND through 20Ω during shutdown.
37	SS	Soft-Start. Connect a 0.01µF to 1µF ceramic capacitor from SS to GND. This capacitor sets the soft-start period during startup. See the *Startup and Soft-Start* section for more details. SS is internally pulled to GND through 20Ω during shutdown.
38	REFIN	External Reference Input. Connect REFIN to AVL to use the internal 0.7V reference for the feedback threshold.

Pin Description (continued)

PIN	NAME	FUNCTION
40	ILIM2	Programmable Current-Limit Input. Connect a resistor from ILIM2 to GND to set the valley current limit. See the *Setting the Current Limit* section.
41	SCOMP	Programmable Slope-Compensation Input. Internal slope-compensation voltage rate is the voltage at SCOMP times 0.1 divided by the oscillator period (T). Connect SCOMP to AVL or GND to set to the default of 250mV/T or 125mV/T, respectively.
43	POK	Open-Drain Power-OK Output. POK goes high impedance when the output voltage rises above 91% of the nominal regulation voltage. POK pulls low during shutdown or when the output drops below 88% of the nominal regulation voltage.
44	FSYNC	Frequency Set and Synchronization Input. Connect a resistor from FSYNC to GND to set the switching frequency, or drive with a clock signal to synchronize between 160kHz and 1.2MHz. See the *Switching Frequency and Synchronization* section.
45	MODE	Current-Limit Operating Mode Selection. Connect MODE to AVL for latch-off current limit or connect MODE to GND for automatic recovery current limit.
46	SYNCO	Synchronization Output. Provides a clock output for synchronizing another MAX8655 with 180° out-of-phase operation.
47	BST	Boost Capacitor Connection. Connect a 0.22µF ceramic capacitor from BST to LXB.
50	LXB	LX Boost Capacitor Connection. Connect a 0.22µF ceramic capacitor between LXB and BST.
—	GND-EP	Exposed Pad. Connect to GND externally. See the *Pin Configuration*.
—	PVIN-EP	Exposed Pad. Internally connected to PVIN. See the *Pin Configuration*.
—	LX-EP	Exposed Pad. Internally connected to LX. See the *Pin Configuration*.

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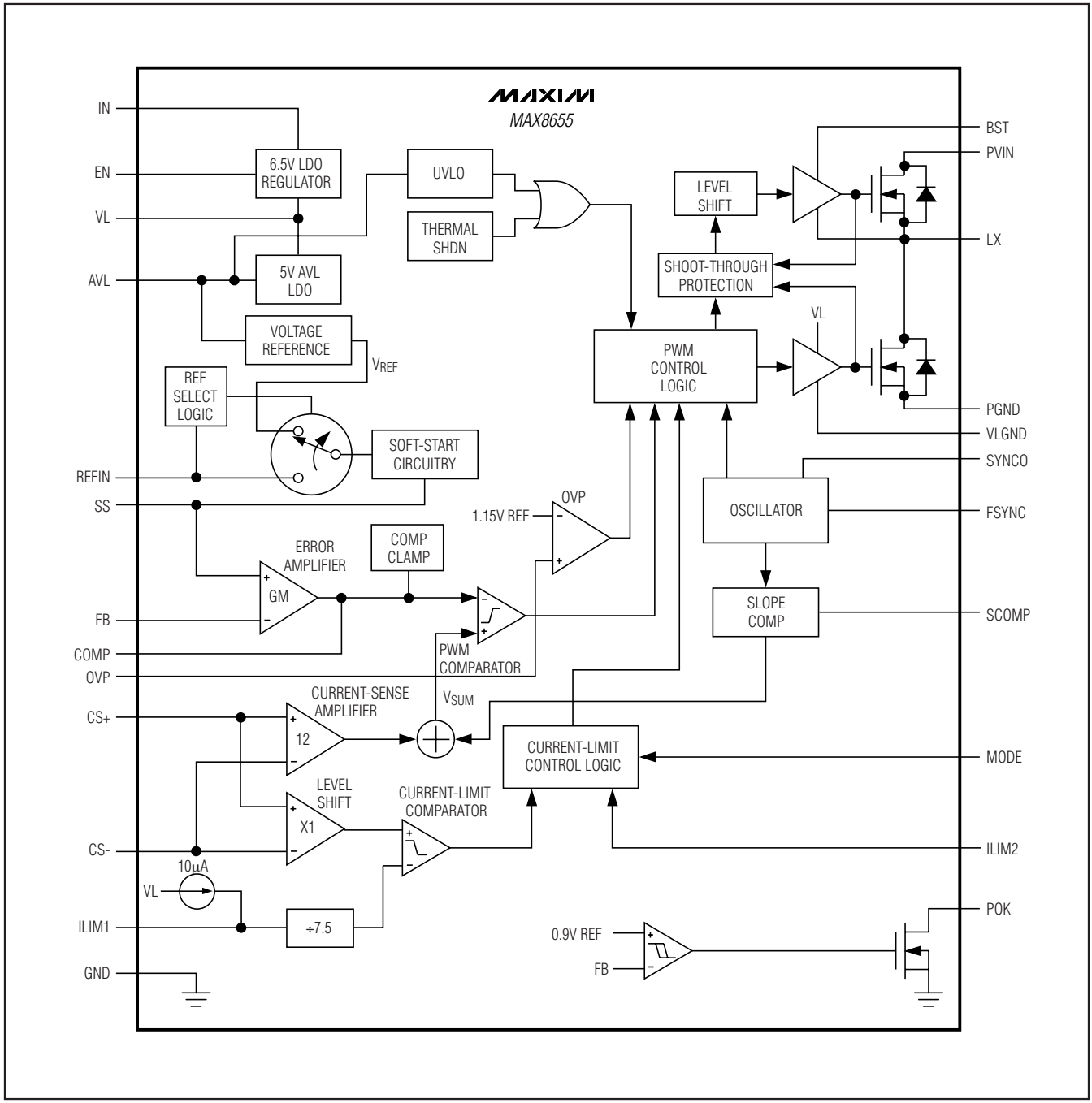

Figure 1. Functional Diagram

Detailed Description

DC-DC Converter Control Architecture

The MAX8655 step-down regulator uses a PWM, peak current-mode control scheme. An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM controller is a PWM comparator that compares the integrated voltage-feedback signal against the amplified current-sense signal plus an adjustable slope-compensation ramp, which is summed with the current signal to ensure stability. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips or the maximum duty cycle is reached. During this on-time, current ramps up through the inductor, storing energy in the output inductor while sourcing current to the output. The current-mode feedback system regulates the peak inductor current as a function of the output-voltage error signal. The circuit acts as a switch-mode transconductance amplifier and pushes the output LC filter pole normally found in a voltage-mode PWM to a higher frequency. Figure 1 is the functional diagram.

During the second half of the cycle, the internal high-side MOSFET turns off and the internal low-side MOSFET turns on. The output inductor releases the stored energy as the current ramps down, providing current to the load. The output capacitor stores charge when the inductor current exceeds the required load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under soft-overload conditions, when the peak inductor current exceeds the selected current limit (see the *Current-Limit Circuit* section), the high-side MOSFET is turned off immediately and the low-side MOSFET is turned on and remains on to let the inductor current ramp down until the next clock cycle. Under severe-overload or short-circuit conditions, the valley foldback current limit is enabled to reduce power dissipation of external components.

The MAX8655 operates in a forced-PWM mode. As a result, the regulator maintains a constant switching frequency, regardless of load, to allow for easier filtering of the switching noise.

Internal Linear Regulators

The MAX8655 contains two internal LDO regulators. The AVL regulator provides 5V for the IC's internal circuitry, and the VL regulator provides 6.5V for the MOSFET gate drivers. Connect a 2.2µF ceramic capacitor from VL to VLGND, and connect a 1µF ceramic capacitor from AVL to GND. The AVL regulator input is internally connected to the VL regulator output. For 5V input applications, connect VL directly to IN and connect a 10Ω resistor from VL to AVL.

Undervoltage Lockout

When V_{AVL} drops below 4.03V, the MAX8655 assumes that the supply voltage is too low to make valid decisions, so the undervoltage-lockout (UVLO) circuitry inhibits switching and turns off both internal power MOSFETs. When V_{AVL} rises above 4.15V, the regulator enters the startup sequence and then resumes normal operation.

Startup and Soft-Start

The internal soft-start circuitry gradually ramps up the reference voltage to control the rate of rise of the output voltage and reduce input surge currents during startup. The soft-start period is determined by the value of the capacitor from SS to GND. The soft-start time is approximately (30.4ms/µF) x C_{SS}. The MAX8655 also features monotonic output-voltage rise; therefore, both power MOSFETs are kept off if the voltage at FB is higher than the voltage at SS. This allows the MAX8655 to start up into a prebiased output without pulling the output voltage down.

Before the MAX8655 begins the soft-start and power-up sequence, the following conditions must be met:

- V_{AVL} exceeds the 4.15V UVLO threshold.
- EN is at logic-high.
- The thermal limit is not exceeded.

Enable

The MAX8655 features a low-power shutdown mode. A logic-low at EN shuts down the regulator. During shutdown, the output is high impedance. Shutdown reduces the IN current to less than 10µA. A logic-high at EN enables the regulator.

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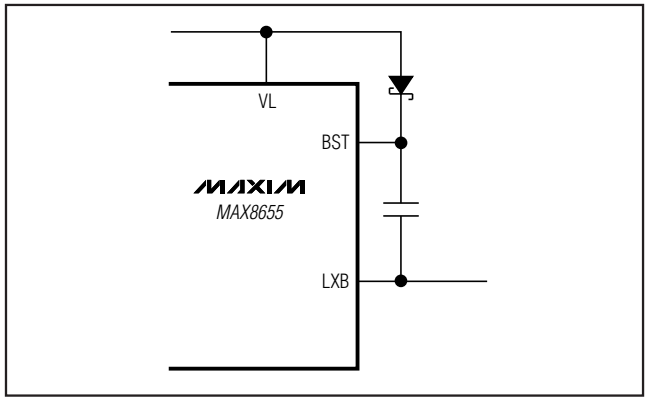

Figure 2. High-Side Gate Boost Circuit

High-Side Gate-Drive Supply (BST)

A flying capacitor boost circuit (Figure 2) generates the gate-drive voltage for the internal high-side n-channel MOSFET. The capacitor between BST and LXB is charged from VL to 6.5V minus the diode forward-voltage drop while the low-side MOSFET is on. When the low-side MOSFET is switched off, the stored voltage of the capacitor is stacked above LXB to provide the necessary turn-on voltage (V_{GS}) for the high-side MOSFET. An internal switch between BST and the internal high-side MOSFET's gate closes to turn the MOSFET on.

Current-Sense Amplifier

The current-sense circuit amplifies the differential current-sense voltage (V_{CS+} - V_{CS-}). This amplified current-sense signal and the internal-slope-compensation signal are summed (V_{SUM}) together and fed into the PWM comparator's inverting input. The PWM comparator shuts off the high-side MOSFET when V_{SUM} exceeds the integrated feedback voltage (V_{COMP}).

The differential current sense is also used to provide peak inductor current limiting. This current limit is more accurate than the valley current limit, which is measured across the internal low-side MOSFET.

Current-Limit Circuit

The MAX8655 uses both foldback and peak current limiting. The valley foldback current limit is used to reduce power dissipation of external components—mainly the inductor, internal power MOSFETs, and the upstream power source, when the output is severely overloaded or short circuited and when POK is low. Thus, the circuit can withstand short-circuit conditions continuously without causing overheating of any component. The peak constant current limit sets the current-limit point more accurately since it does not have to suffer the wide variation of the low-side power MOSFET's on-resistance due to tolerance and temperature.

The valley current is sensed across the on-resistance of the low-side MOSFET. The valley current limit trips when the sensed current exceeds the valley current limit.

Set the minimum valley current limit when the output voltage is at its nominal regulated value, higher than the maximum peak current-limit setting. With this method, the current-limit point accuracy is controlled by the peak current limit and is not interfered with by the wide variation of the MOSFET's on-resistance. See the *Setting the Current Limit* section for how to set these limits.

The MAX8655 can be configured for either an adjustable valley current-limit threshold with adjustable foldback ratio or a fixed valley current limit that latches the regulator off. To use foldback current limit with autorecovery, connect MODE to GND. When the latch-off mode is used, connect MODE to AVL and set the current-limit threshold with one resistor from ILIM2 to GND. Cycle EN or input power to reset the current-limit latch.

The peak current limit is used to sense the inductor current, and is more accurate than the valley current limit because it does not depend upon the on-resistance of the low-side MOSFET. The peak current can be measured across the resistance of the inductor for the highest efficiency, or alternatively, a current-sense resistor can be used for more accurate current sensing. A resistor connected from ILIM1 to GND sets the peak current-limit threshold.

For more information on the current limit, see the *Setting the Current Limit* section.

Switching Frequency and Synchronization

The MAX8655 has an adjustable internal oscillator that can be set to any frequency from 200kHz to 1MHz. To set the switching frequency, connect a resistor from FSYNC to GND.

The MAX8655 can also be synchronized to an external clock by connecting the clock signal to FSYNC. A synchronization output (SYNCO) is provided to synchronize a second MAX8655 180° out-of-phase with the first by connecting SYNCO of the first MAX8655 to FSYNC of the second. When the first MAX8655 is synchronized to an external clock, the external clock is inverted to generate SYNCO. Therefore, to get 180° out-of-phase operation with an external clock, the clock input to the first MAX8655 should have a 50% duty cycle. Figure 3 is the single-phase, 600kHz switching, 10.8V to 13.2V input and 1.2V/20A output. Figure 4 shows single-phase, 350kHz switching, 6V to 20V input, and 3.3V/20A output.

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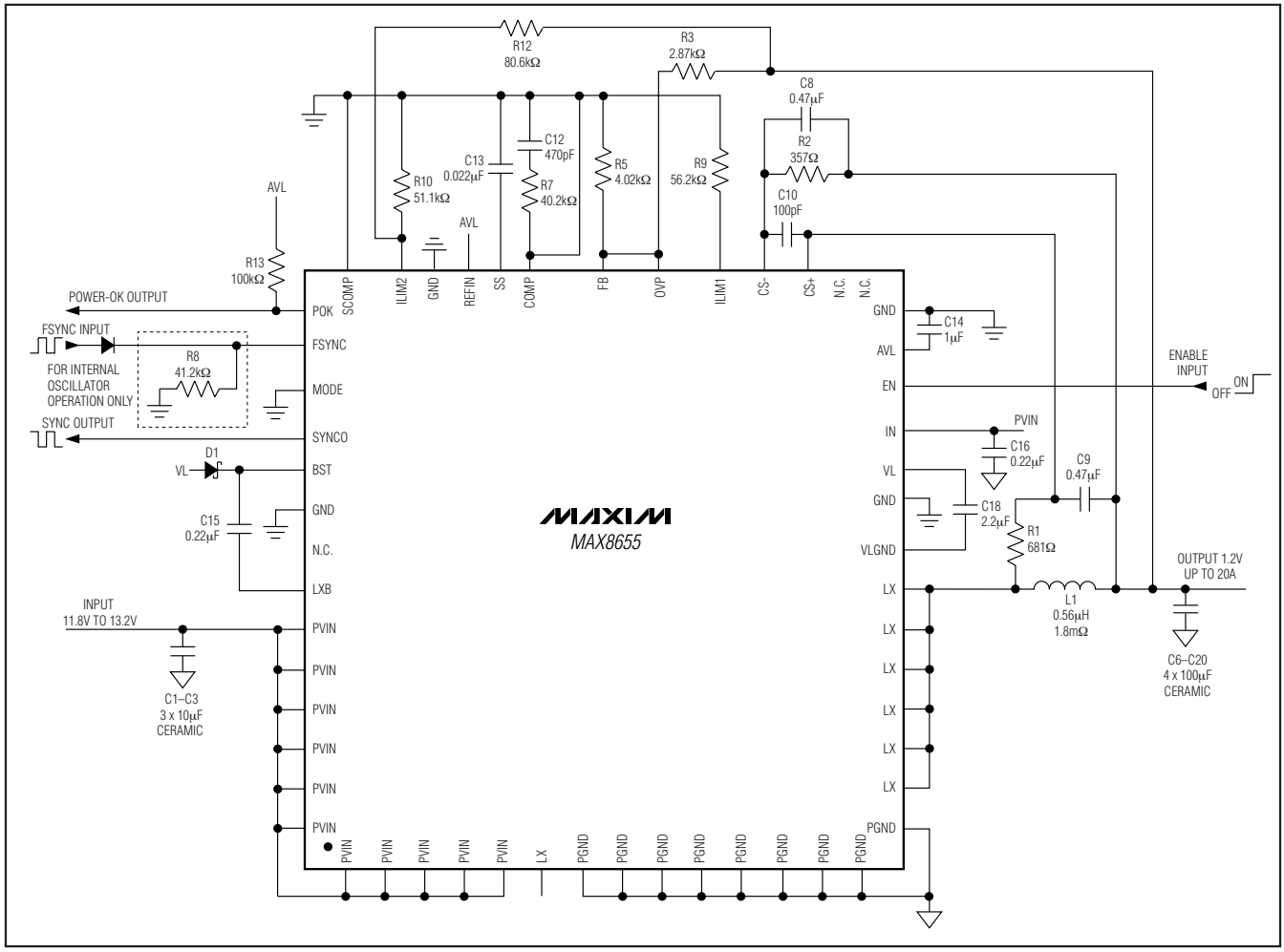

Figure 3. Single-Phase, 600kHz Switching, 10.8V to 13.2V Input, and 1.2V/20A Output

REFIN

The MAX8655 has a reference input (REFIN). When an external reference up to 1.5V is connected to REFIN, the feedback regulation voltage is equal to the voltage applied to REFIN.

Connect REFIN to AVL to use the internal 0.7V reference.

Overvoltage Protection

The MAX8655 provides output overvoltage protection (OVP). The OVP threshold is set independent of the output regulation voltage with a resistor voltage-divider. When the voltage at OVP exceeds the OVP threshold, the regulator stops switching and latches on the low-side power MOSFET. Cycle EN or the power applied to AVL to clear the latch.

Power-Good Signal (POK)

POK is an open-drain output on the MAX8655 that monitors the output voltage. When the output is above 92% of its nominal regulation voltage, POK is high impedance. When the output drops below 89% of its nominal regulation voltage, POK is internally pulled low. POK is also internally pulled low when the MAX8655 is shut down or in a fault condition.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8655. When the junction temperature exceeds +160°C, an internal thermal sensor shuts down the device, allowing the IC to cool. The thermal sensor turns the IC on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

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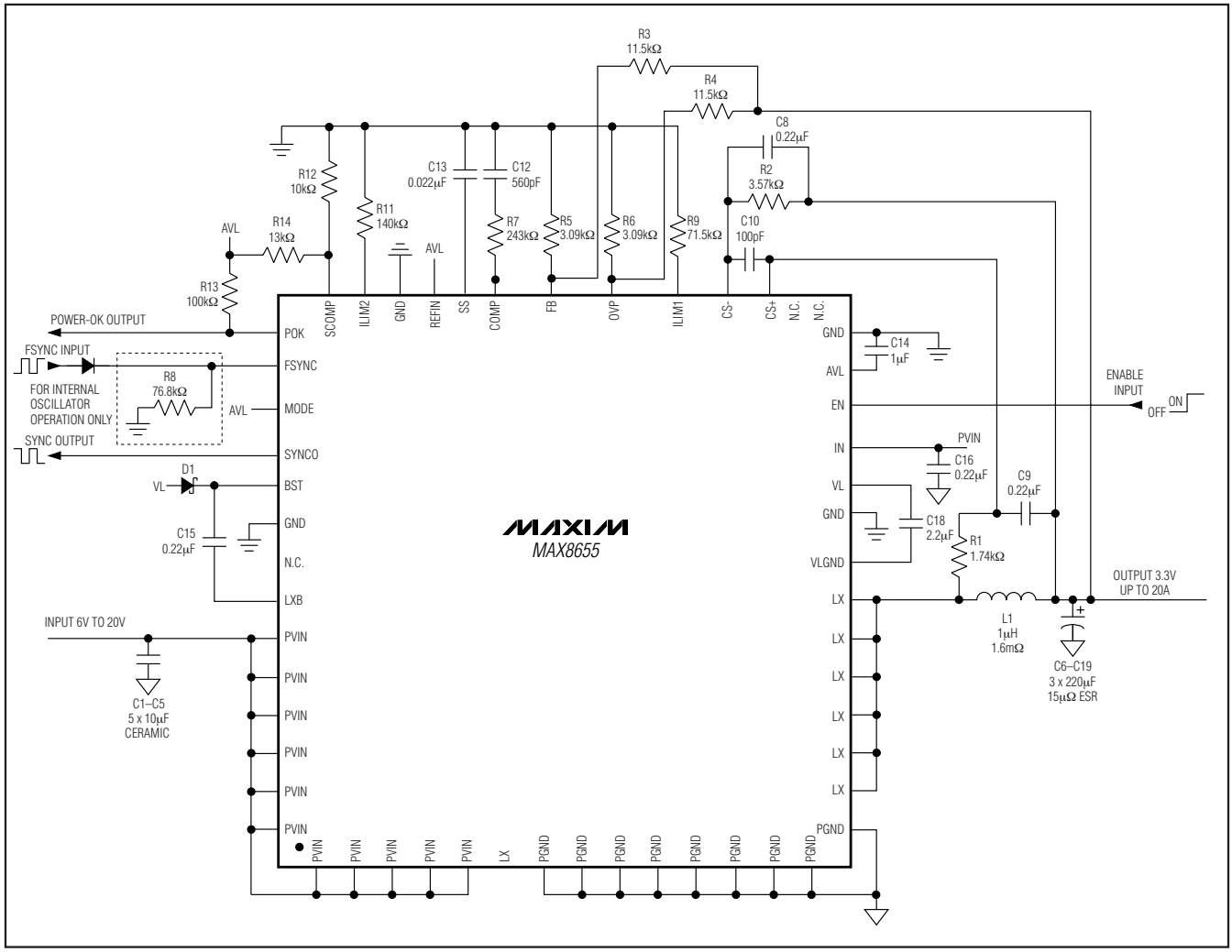

Figure 4. Single-Phase, 350kHz Switching, 6V to 20V Input, and 3.3V/20A Output

Design Procedure

Setting the Output Voltage

To set the output voltage for the MAX8655, connect FB to the center of an external resistor-divider from the output to GND (R3 and R5 of Figure 5). Select R5 between 5kΩ and 24kΩ, and then calculate R3 with the following equation:

$$R3 = R5 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 0.7V or V_{REFIN}. R3 and R5 should be placed as close as possible to the IC.

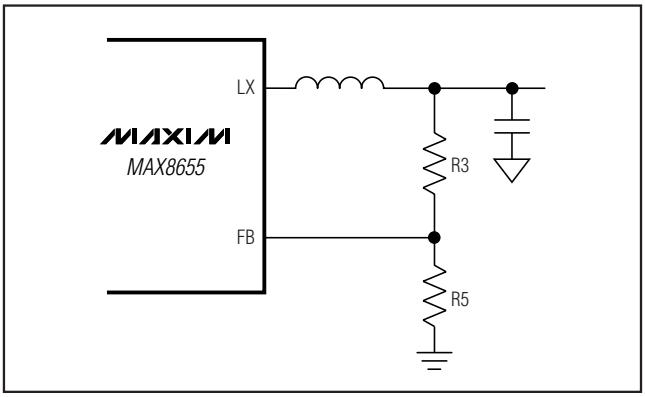

Figure 5. Setting the Output Voltage with a Resistor Voltage-Divider

Setting the Output Overvoltage Protection

To set the overvoltage threshold voltage for the MAX8655, connect OVP to the center of an external resistor-divider connected between the output and GND (R4 and R6 of Figure 3). Select R6 between 5kΩ and 24kΩ, then calculate R4 with the following equation:

$$R4 = R6 \times \left(\frac{V_{OUT}}{V_{OVP}} - 1 \right)$$

where $V_{OVP} = 1.15 \times V_{FB}$.

Inductor Selection

There are several parameters that must be examined when determining which inductor is to be used. Input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of the inductor current ripple to the maximum DC load current. A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple. A good compromise between size and efficiency is an LIR of 0.3. Once all the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

where f_S is the switching frequency. Choose a standard-value inductor close to the calculated value. The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. This is especially true if the inductance is increased without also increasing the physical size of the inductor. Find a low-loss inductor having the lowest possible DC resistance that fits the allotted dimensions. The chosen inductor's saturation current rating must exceed the peak inductor current determined as:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{LIR}{2} \times I_{LOAD(MAX)}$$

Setting the Switching Frequency

To set the switching frequency, connect a resistor from FSYNC to GND. Calculate the resistor value in kΩ from the following equation:

$$R_{FSYNC} = \frac{30600}{f_S} - 9.914$$

where f_S is the desired switching frequency in kHz.

Setting the Slope Compensation

For most applications where the duty cycle is less than 40%, connect SCOMP to GND to set the internal slope compensation to the default of 125mV/T, where T is the oscillator period ($T = 1 / f_S$).

For a slope compensation of 250mV/T, connect SCOMP to AVL.

For applications with a duty cycle greater than 40%, set the SCOMP voltage with a resistor voltage-divider from AVL to GND (R11 and R12 in Figure 6). First, use the following equation to find the SCOMP voltage:

$$V_{SCOMP} = \frac{120 \times R_L}{f_S \times L} \times (V_O - 0.182 \times V_{IN\_MIN})$$

where R_L is the DC resistance of the inductor, V_{IN_MIN} is the minimum operating input voltage, and f_S is the switching frequency.

Next, select a value for R11, typically 10kΩ, and solve for R12 as follows:

$$R12 = \frac{(5V - V_{SCOMP}) \times R11}{V_{SCOMP}}$$

This sets the internal slope-compensation voltage rate to $V_{SCOMP} / (10 \times T)$.

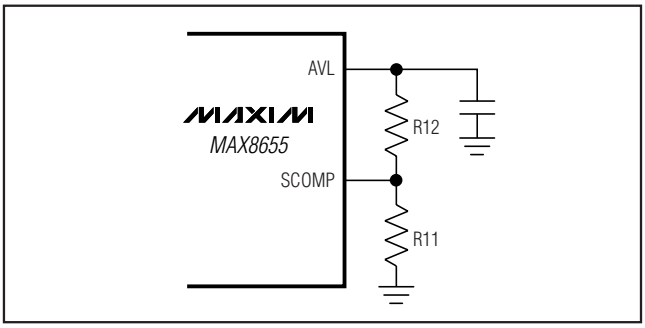

Figure 6. Resistor-Divider for Setting the Slope Compensation

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Setting the Current Limit

Valley Current Limit

The MAX8655 has an adjustable valley current limit, configurable for foldback with automatic recovery, or constant-current limit with latch-up. To set the constant-current limit for the latch-up mode, connect a single resistor R_{ILIM2} from ILIM2 to GND. For latch-up current-limit mode, set R_{ILIM2} equal to R_{VALLEY} obtained from the R_{VALLEY} vs. Valley Current Limit graph in the *Typical Operating Characteristics* section for the required valley current I_{VALLEY}. I_{VALLEY} is the value of the inductor valley current at maximum load ($I_{LOAD(MAX)}$ - $1/2$ I_{P-P})

To set the current limit for foldback mode, connect a resistor from ILIM2 to the output (R_{FOBK}), and another resistor from ILIM2 to GND (R_{ILIM2}). See Figure 7. The values of R_{FOBK} and R_{ILIM2} are calculated as follows.

First, select the percentage of foldback (P_{FB}). This percentage corresponds to the current limit when V_{OUT} equals zero divided by the current limit when V_{OUT} equals its nominal voltage. A typical value of P_{FB} is in the 15% to 40% range. A lower value of P_{FB} yields lower short-circuit current. The following equations are used to calculate R_{FOBK} and R_{ILIM2}:

$$R_{FOBK} = \frac{P_{FB} \times V_{OUT}}{I_{ILIM2} \times (1 - P_{FB})}$$

$$R_{ILIM2} = \frac{I_{ILIM2} \times R_{VALLEY} \times R_{FOBK}}{V_{OUT} + (I_{ILIM2} \times (R_{FOBK} - R_{VALLEY}))}$$

where I_{ILIM2} is 5µA.

If the resulting value of R_{ILIM2} is negative, increase P_{FB}.

Peak Current Limit

The peak current-limit threshold (V_{TH}) is set by a resistor connected from ILIM1 to GND (R_{ILIM1}). V_{TH} corresponds to the peak voltage across the sensing element (inductor or current-sense resistor). R_{ILIM1} is calculated as follows:

$$R_{ILIM1} = \frac{7.5 \times V_{TH}}{10\mu A}$$

This allows a maximum DC output current of:

$$I_{LIM} = \frac{V_{TH}}{R_L} - \frac{I_{P-P}}{2}$$

where R_L is the DC resistance of the inductor.

To ensure maximum output current, use the minimum value of V_{TH} from each setting, and the maximum R_L values at the highest expected operating temperature. The DC resistance of the inductor's copper wire has a +0.38%/°C temperature coefficient.

An RC circuit is connected across the inductor (see Figure 8). The RC time constant is set to be 1.1 to 1.2 times the inductor (L/R_L) time constant. Pick the value of C9 in the 0.1µF to 0.47µF range, and then calculate R1 from:

$$R1 = 1.2L / (R_L \times C9)$$

Add a resistor (R2 in Figure 8) to the CS- connection to minimize input offset error. Calculate the value of R2 as follows:

• When $V_{OUT} \geq 2.4V$:

$$R2 = \frac{\left(20\mu A + \frac{R_{ILIM1} \times 10\mu A}{32k\Omega}\right) \times R1}{20\mu A}$$

• When $V_{OUT} < 2.4V$:

$$R2 = \frac{15\mu A \times R1}{\left(15\mu A + \frac{R_{ILIM1} \times 10\mu A}{32k\Omega}\right)}$$

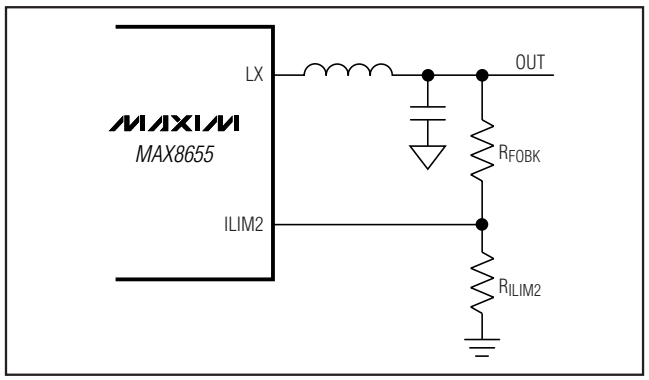

Figure 7. ILIM2 Resistor Connections

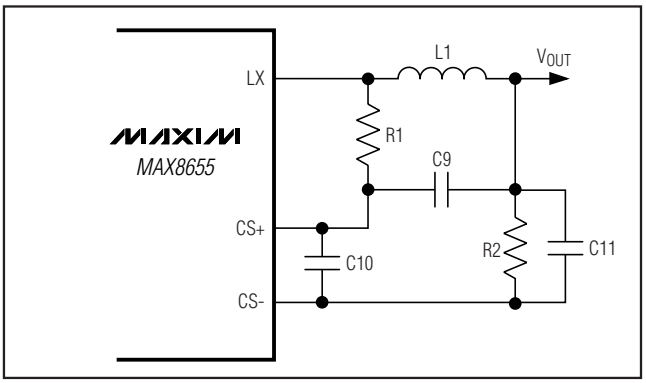

Figure 8. Current Sense Using the Inductor's DC Resistance

Capacitor C11 is connected in parallel with R2 and is equal in value with C9.

Add a 100pF (C10) capacitor across the CS+ and CS- inputs close to the IC.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitors must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{I_{LOAD}\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)} = I_{LOAD} / 2$. Ceramic capacitors are recommended due to the low ESR and ESL at high frequency with relatively low cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability. Ceramic capacitors with an X5R or better temperature characteristic are recommended.

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage-rating requirements. These parameters affect the overall stability, output-voltage ripple, and transient response. The output ripple has three components: variations in the charge stored in the output capacitor, the voltage drop across the capacitor's ESR, and ESL caused by the current into and out of the capacitor. The maximum output-voltage ripple is estimated as follows:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

The output-voltage ripple as a consequence of the ESR, ESL, and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN}}{L + ESL} \times ESL$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

where I_{P-P} is the peak-to-peak inductor current.

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

These equations are suitable for initial capacitor selection, but final values should be chosen based on a prototype or evaluation circuit. As a general rule, a smaller current ripple results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value and input voltage, the output-voltage ripple decreases with larger inductance, and increases with higher input voltages. The MAX8655 is designed to work with polymer, tantalum, aluminum electrolytic, or ceramic output capacitors. The aluminum electrolytic capacitor is the least expensive; however, it has higher ESR. To compensate for this, use a ceramic capacitor in parallel to reduce the switching ripple and noise. Ceramic capacitors are recommended for high-frequency (500kHz to 1MHz) designs. For reliable and safe operation, ensure that the capacitor's voltage and ripple-current ratings exceed the calculated values.

The response to a load transient depends on the selected output capacitors. During a load transient, the output voltage instantly changes by ESR x ΔI_{LOAD}. Before the regulator can respond, the output voltage deviates further, depending on the inductor and output-capacitor values. After a short time (see the *Typical Operating Characteristics* section), the regulator responds by regulating the output voltage back to its nominal state. The regulator response time depends on its closed-loop bandwidth. With a higher bandwidth, the response time is faster, thus preventing the output voltage from further deviation from its regulating value.

Compensation Design

The MAX8655 uses an internal transconductance error amplifier whose output compensates the control loop. The external inductor, output capacitor, compensation resistor, and compensation capacitors determine the loop stability. The inductor and output capacitor are chosen based on performance, size, and cost. Additionally, the compensation resistor and capacitors are selected to optimize control-loop stability. The component values, shown in Figures 3 and 4, yield stable operation over the given range of input-to-output voltages.

The regulator uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The voltage drop across the DC resistance of the inductor or the alternate series current-sense resistor is used to measure the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the

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inductor and output capacitor resulting in a smaller phase shift and requiring a less elaborate error-amplifier compensation than voltage-mode control. A simple series R_C and C_C is all that is needed to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering. For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output-capacitor loop, add another compensation capacitor from COMP to GND to cancel this ESR zero. See Figure 9.

The basic regulator loop is modeled as a power modulator, an output feedback divider, and an error amplifier. The power modulator has DC gain $G_{MOD(dc)}$, set by $g_{mc} \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its equivalent series resistance (ESR). Below are equations that define the power modulator:

$$G_{MOD(dc)} = g_{mc} \times \frac{R_{LOAD}}{\left[1 + \frac{R_{LOAD}}{L \times f_S} \times \left[\left(K_S \times \left(1 - D\right)\right) - 0.5\right]\right]}$$

where $R_{LOAD} = V_{OUT} / I_{OUT(MAX)}$, f_S is the switching frequency, L is the output inductance, $g_{mc} = 1 / (A_{VCS} \times R_L)$, where A_{VCS} is the gain of the current-sense amplifier (12 typ), R_L is the DC resistance of the inductor, the duty cycle $D = V_{OUT} / V_{IN}$. K_S is a slope compensation factor calculated from the following equation:

$$K_S = 1 + \frac{V_{SCOMP} \times L \times f_S}{120 \times (V_{IN} - V_O) \times R_L}$$

When SCOMP is connected to GND, use V_{SCOMP} = 1.25V; when SCOMP is connected to AVL, use V_{SCOMP} = 2.5V.

Find the pole and zero frequencies created by the power modulator as follows:

$$f_{pMOD} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} + \left[\frac{1}{2\pi \times L \times f_S \times C_{OUT}} \times \left[K_S \times (1 - D) - 0.5\right]\right]$$

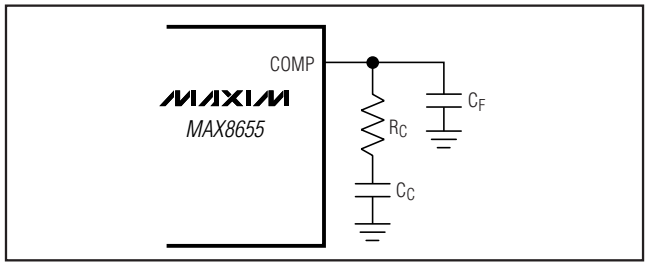

Figure 9. Compensation Components

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

When C_{OUT} comprises "n" identical capacitors in parallel, the resulting C_{OUT} = n x $C_{OUT(EACH)}$, and ESR = $ESR_{(EACH)}$ / n. Note that the capacitor zero for a parallel combination of like capacitors is the same as for an individual capacitor. Figure 10 is the simplified gain plot for the $f_{zMOD} > f_C$ case.

The feedback voltage-divider has a gain of $G_{FB} = V_{FB} / V_{OUT}$, where V_{FB} is equal to 0.7V.

The transconductance error amplifier has a DC gain, $G_{EA(DC)} = g_{mEA} \times R_O$, where g_{mEA} is the error-amplifier transconductance, which is equal to 110µS, and R_O is the output resistance of the error amplifier, which is 30MΩ. A dominant pole (f_{pdEA}) is set by the compensation capacitor (C_C), the amplifier output resistance (R_O), and the compensation resistor (R_C); a zero (f_{zEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C). Thus:

$$f_{pdEA} = \frac{1}{2\pi \times C_C \times (R_O + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

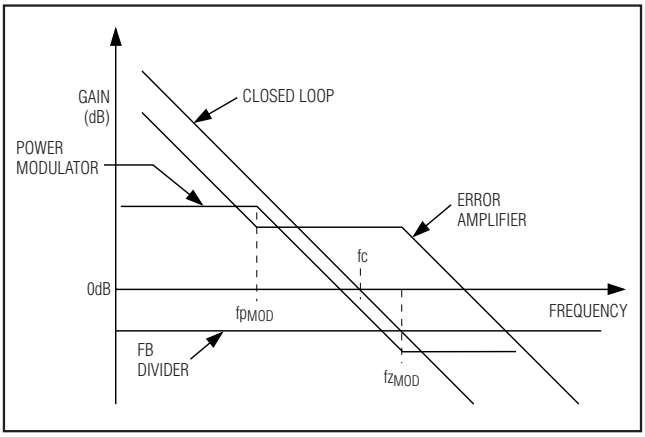

Figure 10. Simplified Gain Plot for the $f_{zMOD} > f_C$ Case

The crossover frequency, f_C, should be much higher than the power-modulator pole f_{PMOD}. Also, f_C should be less than or equal to 1/5 the switching frequency. Select a value for f_C in the range:

$$f_{pMOD} << f_C \le \frac{f_S}{5}$$

At the crossover frequency, the total loop gain must equal 1, and is expressed as:

$$G_{EA(fc)} \times G_{MOD(fc)} \times \frac{V_{FB}}{V_{OUT}} = 1$$

For the case where f_{zMOD} is greater than f_C:

$$G_{EA(fc)} = g_{mEA} \times R_C$$

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Then R_C can be calculated as:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(fc)}}$$

where g_{mEA} = 110µS.

The error-amplifier compensation zero formed by R_C and C_C should be set at the modulator pole f_{PMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor C_F from COMP to GND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

For the case where f_{zMOD} is less than f_C:

The power modulator gain at f_C is:

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at f_C is:

$$G_{EA(fc)} = g_{mEA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

Figure 11 is the simplified gain plot for the $f_{zMOD} < f_C$ case.

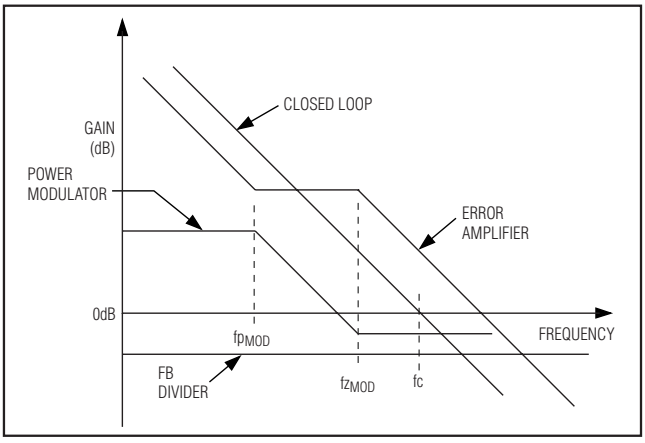

Figure 11. Simplified Gain Plot for the $f_{zMOD} < f_C$ Case

R_C is calculated as:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{f_C}{g_{mEA} \times G_{MOD(fc)} \times f_{zMOD}}$$

where g_{mEA} = 110µS.

C_C is calculated from:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

C_F is calculated from:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

The current-mode control model on which the above design procedure is based requires an additional high-frequency term, $G_S(s)$, to account for the effect of sampling the peak inductor current. The term $G_S(s)$ produces additional phase lag at crossover and should be modeled to estimate the phase margin obtainable by the selected compensation components. As a final step, it is useful to plot the dB gain and phase of the following loop-gain transfer function and check the

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obtained phase margin. A phase margin of at least 45° is recommended:

$$G_{LOOP}(s) = \frac{g_{mc} \times R_{LOAD}}{\left[1 + \frac{R_{LOAD}}{L \times f_S} \times \left[\left(K_S \times (1-D)\right) - 0.5\right]\right]} \times \frac{(1 + s/2\pi \times f_{zMOD})}{(1 + s/2\pi \times f_{pMOD})} \times \frac{(1 + s/2\pi \times f_{zEA})}{(1 + s/2\pi \times f_{pEA}) \times (1 + s/2\pi \times f_{pdEA})} \times \frac{g_{mEA} \times Ro \times V_{FB}}{V_O} G_S(s)$$

$$G_S(s) = \frac{1}{\left(1 + \frac{s}{\pi . Q_C . f_S} + \frac{s^2}{(\pi . f_S)^2}\right)}$$

where the sampling effect quality factor:

$$Q_C = \frac{1}{\left[\pi . (K_S . (1-D) - 0.5)\right]},$$

Below is a numerical example to calculate R_C and C_C values of the typical operating circuit of Figure 3:

A_{VCS} = 12

L = 0.56µH

R_L = 1.8mΩ

f_S = 600kHz

g_{mc} = 1 / (A_{VCS} x R_L) = 1 / (12 x 0.0018) = 46.29S

V_{OUT} = 1.2V

$I_{OUT(MAX)}$ = 20A

R_{LOAD} = V_{OUT} / $I_{OUT(MAX)}$ = 1.2 / 20 = 0.06Ω

C_{OUT} = 4 x 100µF = 400µF

ESR = 2mΩ / 4 = 0.5mΩ

D = V_{OUT} / V_{IN} = 1.2 / 12 = 0.1:

$$K_S = 1 + \frac{V_{SCOMP} \times L \times f_S}{120 \times (V_{IN} - V_O) \times R_L} = 1 + \frac{1.25(0.56 \times 10^{-6})(600000)}{120(12 - 1.2)(0.0018)} = 1.18$$

$$G_{MOD(dc)} = g_{mc} \times \frac{R_{LOAD}}{\left[1 + \frac{R_{LOAD}}{L \times fs} \times \left[\left(K_S \times (1-D)\right) - 0.5\right]\right]} = 46.29 \times \frac{0.06}{1 + \frac{0.06}{(0.56 \times 10^{-6})(600000)} \times \left[1.18(1-0.1) - 0.5\right]} = 2.53$$

$$f_{pMOD} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT} \times 0.9} + \left[\frac{1}{2\pi \times L \times f_S \times C_{OUT} \times 0.8} \times \left[K_S \times (1-D) - 0.5\right]\right] = \frac{1}{2\pi(400 \times 10^{-6})(0.06) \times 0.9} + \left[\frac{1}{2\pi(0.56 \times 10^{-6})(600000)(400 \times 10^{-6}) \times 0.8} \left(1.18(1-0.1) - 0.5\right)\right] = 8.18kHz$$

$$f_{pMOD} << f_C \le \frac{f_S}{5}$$

8.18kHz << f_C ≤ 120kHz, select f_C = 60kHz.

$$f_{zMOD} = \frac{1}{2\pi \times 0.9 \times C_{OUT} \times ESR} = \frac{1}{2\pi \times 0.9 \times (400 \times 10^{-6}) \times 0.0005} = 884.2kHz$$

Since f_{zMOD} > f_C:

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_c} = 2.53 \times \frac{8118}{60000} = 0.345$$

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{1}{g_{mEA} \times G_{MOD(fc)}} = \frac{1.2}{0.7} \times \frac{1}{(110 \times 10^{-6})(0.307)}$$

R_C = 44.7kΩ

Select the nearest standard value: R_C = 40.2kΩ:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C} = \frac{1}{2\pi \times 8181 \times (40.2 \times 10^3)} = 483.9pF$$

Select the nearest standard value: C_C = 470pF:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}} = \frac{1}{2\pi \times (40.2 \times 10^3) \times (884.2 \times 10^3)} = 5pF$$

R7 = R_C = 40.2kΩ

C12 = C_C = 470pF

C11 = C_F = 5pF (not used)

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low losses and clean, stable operation. Refer to the MAX8655 Evaluation Kit for an example layout. If it is necessary to deviate from this layout, follow the procedure below. Follow these guidelines for good PCB layout:

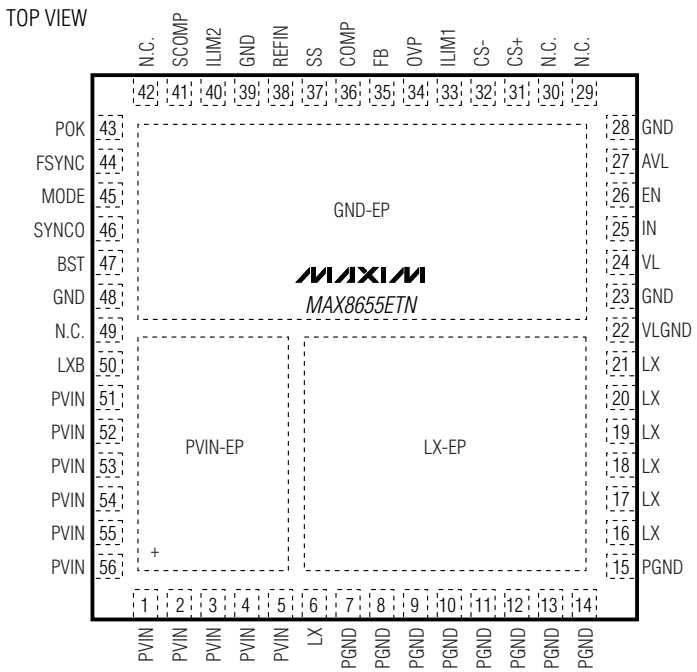
1) Place IC decoupling capacitors as close as possible to the IC pins. Separate the power and analog ground planes. Place the input ceramic decoupling capacitor directly across and as close as possible to PVIN and PGND. This is to help contain the high switching current within this small loop.
2) For output current greater than 10A, a four-layer PCB is recommended. Pour an analog ground plane in the second layer underneath the IC to minimize noise coupling.
3) Connect input, output, and VL capacitors to the power ground plane; connect all other capacitors to the signal ground plane. Connect analog and power ground planes at the output capacitor.
4) Place the inductor current-sense resistor and capacitor as close as possible to the inductor. Make a Kelvin connection to minimize the effect of PCB trace resistance. Place the input bias balance resistor (R2 in Figure 8) near CS-. Run two closely parallel traces from across capacitor C9 to CS+ and the input bias balance resistor R2.
5) Connect the exposed pad sections to the corresponding IC pins and allow sufficient copper area to help cooling the device.
6) Place the feedback and compensation components as close as possible to the IC pins. Connect the feedback resistor-divider from FB to V_{OUT} as close as possible to the farthest output capacitor.

Chip Information

PROCESS: BiCMOS

Highly Integrated, 25A, Wide-Input, Internal MOSFET, Step-Down Regulator

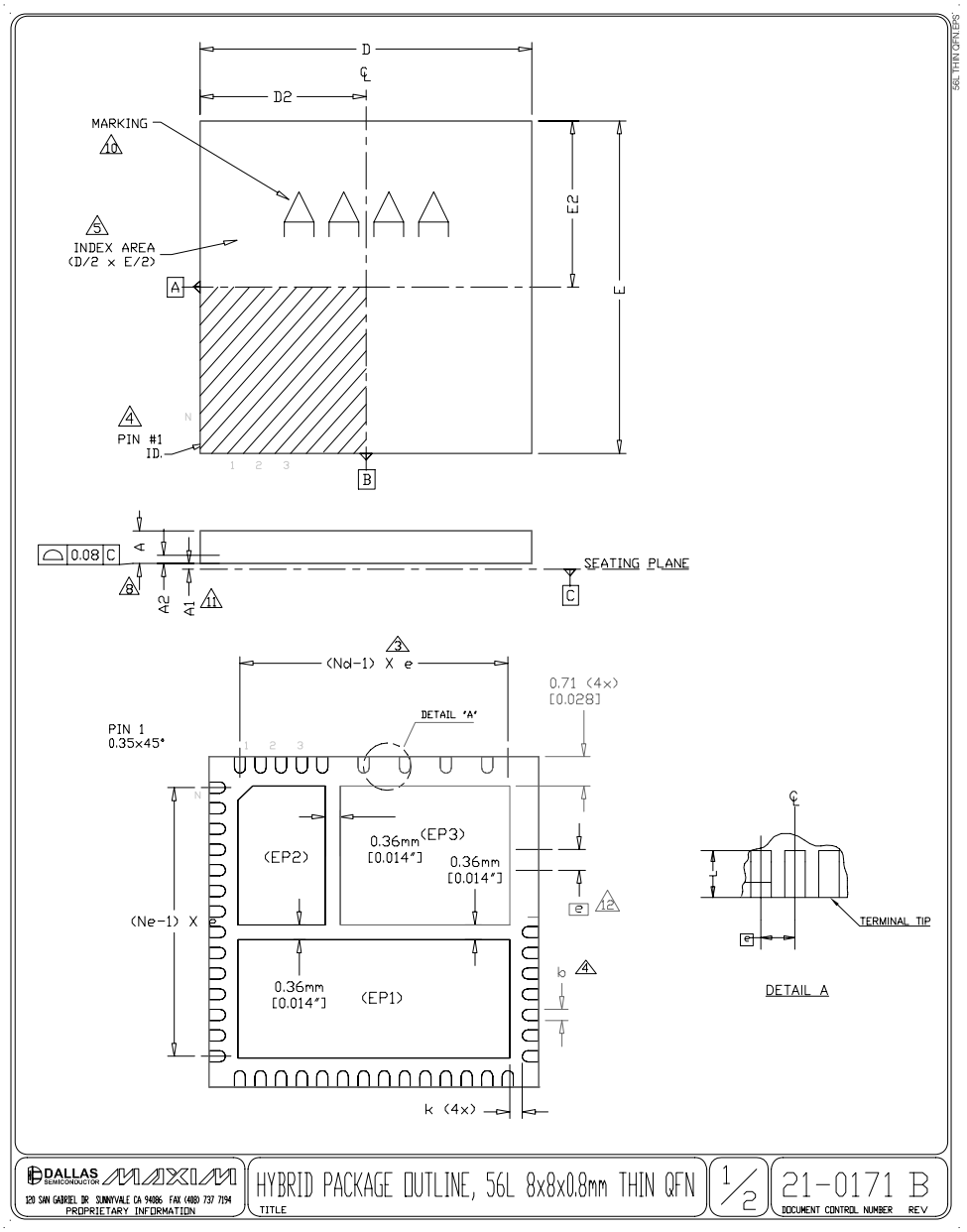
Pin Configuration



THIN QFN
(8mm x 8mm)

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Highly Integrated, 25A, Wide-Input, Internal MOSFET, Step-Down Regulator

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS			
PKG.	T5688M-4		
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20 REF.	
b	0.20	0.25	0.30
D	7.90	8.00	8.10
D2	3.95	4.00	4.05
E	7.90	8.00	8.10
E2	3.95	4.00	4.05
e		0.50 BSC.	
k	0.25	-	-
L	0.30	0.40	0.50
ND		14	
NE		14	

EXPOSED PAD VARIATIONS		
SYMBOL	MILLIMETER	INCH
EP1	6.59x2.87	0.259x0.113
EP2	2.11x3.37	0.083x0.133
EP3	4.12x3.37	0.162x0.133

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. WARPAGE SHALL NOT EXCEED 0.10 mm.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. DIMENSION "A1" IS BASE ON EMBOSSING OF THE LEAD SURFACES.
12. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY DIMENSION "e", ±0.05.
13. UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE ±0.05mm EXECPT DIMENSION "k."

DALLAS SEMICONDUCTOR MAXIM
120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

TITLE: HYBRID PACKAGE OUTLINE, 56L 8x8x0.8mm THIN QFN

2/2

DOCUMENT CONTROL NUMBER: 21-0171 B

REV